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09/891,578	06/25/2001	Jun Kim	RAMB-01067US0	3316

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EXAMINER	
CHANG, EDITH M	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,578	KIM ET AL.	
	Examiner	Art Unit	
	Edith M. Chang	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 7, 2006 has been entered.

Response to Arguments

2. Applicant's arguments filed February 7, 2006 have been fully considered but they are not persuasive.

Argument: Regarding claims 15 & 18, Applicants argue that there are no illustrations in APA Fig.2 or description in the Background of clock signals CLK1 and CLK2 "having different propagation delays...".

Response: Fig.2 of APA is the background of the invention disclosed in Fig.3 of the current application, wherein CLK1 having PHASE1 and CLK2 having PHASE2 illustrate and describe the clock signals having different propagation delays which are caused by the control values PHASE1 and PHASE2, and can be caused by the layout/structure of the device as well (this is well-known in the art) shown in Fig.1 and Fig.2.

Argument: Regarding claim 1, Applicants argue that APA Fig.2 Phase detection circuit 31 compares clock signals CLK1 and CLK2 to determine whether the phase of CLK2 relative to CLK1 is greater than 90 degree (Application, page 3, lines 7-8).

Response: APA Fig.2 and Application, page 3, lines 7-8 disclose that the Phase detection circuit 31 comparing the phase (value) of CLK1 and CLK2 to detect a phase relationship (whether the phase of CLK2 relative to CLK1 is greater 90 degree) between the first (CLK1) and second clock (CLK2) signals *as recited in the claim.*

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 4 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 9 with its method (claim 4) is not described or disclosed in drawings Fig.3 of a clock synchronization circuit and Fig.4 of a phase detection circuit (page 4, lines 6-9, the specification). Since claim 9, inhering the limitations of claim 6, is the device shown in Fig.3, comprising a first clock generator 44; a second clock generator 45; a

phase detection logic 60; and as recited in claim 9 further comprising a calibration logic to receive a third clock signal and to set the second digital control value (PHASE1 or PHASE2).

If the latching logic 64 of Fig.3 is the further calibration logic to receive a third clock signal (DATAIN), the latching logic 64 does not set the PHASE2 (or PHASE1) as recited in the claim, wherein the PHASE2 is set by CAL LOGIC 52 (the PHASE 1 set by CAL LOGIC 50).

If claim 9 is the device shown in Fig.3 with the phase detection (60) shown in Fig.4, how does the Phase detection 60 of Fig.4 with input from the F/F 74 and output to Clock Gen 73 implement the Phase detection 60 of Fig.3 having only inputs PHASE1, PHASE2, and output 62 detect signal to the Latching logic 64.

Hence the claim(s) contains subject matter which do not describe in the specification (i.e. shown in the disclosure of drawings) in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1, 3, 6, 8, and 25-47 are rejected under 35 U.S.C. 102(a) as being anticipated by admitted prior art (APA).

Regarding **clams 1** & **6**, APA Fig.2 discloses a device comprising:

a first clock generator (20 & 22) receiving a first digital control value (PHASE1) to generate a first clock signal (CLK1);

a second clock generator (20 & 23) receiving a second digital control value (PHASE2) to generate a second clock signal (CLK2); and

a phase detection logic (31) comparing CLK1 and CLK2 to detect a phase relationship between the first and second clock signals (page 3, lines 6-8, the specification).

> In Specification, page 3, lines 6-8, the phase relationship is whether the phase of CLK2 relative to CLK1 is greater than 90 degree.

Regarding **claims 3** & **8**, in Fig.2, the APA discloses

a calibration logic element 22 with PHASE1 setting to set the first clock signal (CLK1) having the phase of PHASE1 value;

an input latch (flip/flop element 25) clocked by the first clock signal CLK1 to latch the received data signal (DATAIN) to produce the captured data CDATA; and

a latching logic (elements 26 and 27) latching CDATA to produce the synchronized data signal SDATA in response to the signal on line 30 from the phase detection element 31, therefore the APA discloses the invention recited in the claims.

Regarding **claims 25**, **34** & **41**, in Fig.2, the APA discloses a device and its method, the device comprises

an input clock generator (a clock generator generating the input timing signal CLK1) with the setting PHASE1 value related to a target timing signal (CLK2) generated with reference source element 20 by setting a phase control value (PHASE2),

an input latch (25) clocked by the input clock signal (CKL1) to latch the received signal DATAIN and to produce a captured data CDATA;

an evaluation logic (the phase detection circuit element 31) to evaluate and compare the phase values of the two clock signals CLK1 and CLK2 (lines 7-10, page 3, the specification) to produce a detect signal on line 30 to determine a timing phase to clock the captured data signal (CDATA);

a latching logic (26) to latch and to clock by the timing phase (27) the captured data (CDATA) to produce a synchronized data signal (SDATA) relative to the target timing signal (CK2) provided by a clock generator 23 setting the phase control value to PHASE2.

Regarding **claims 26-27**, **35-36** & **43-44**, in Fig.2, the APA discloses the phase detection circuit element 31 comparing the PHASEI of CLKI to a reference value represents a 90 degree phase offset/lead from the CLK2 (elements 33 & 31), wherein the element 33 delays the CLKI comparing to CLK2.

Regarding **claims 28-30, 40** & **42**, the APA discloses the phase detection circuit element 31 comparing the PHASE1 of CLK1 (the input phase of the input timing signal) to PHASE2 of CLK2 (the target phase of the target timing signal), wherein the CLK2 is generated in response of the set PHASE2 and CLK1 is generated in response of the set

PHASE 1.

Regarding **claims 31, 37 & 45**, the APA device or method discloses that the phase value is a digital value.

Regarding **claims 32, 38 & 46**, in Fig.2 and page 3 lines 6-12 of the current application, the APA teaches the element 31 determines the timing phase to clock the CDATA, the timing phase to be the CLK2 (choosing the element 26a) if CLK2 lags CLKI more than 90 degree, to be the complement of CLK2 (180 degree relative to the CLKZ, choosing the element 26b) if CLK2 lags CLK1 less than 90 degree.

Regarding **claims 33, 39 & 47**, in Fig.2, the APA teaches the latch element 24 clocking the synchronized data signal SDATA with CLK2 the target timing signal.

7. Claims 11-12 and 13-14 are rejected under 35 U.S.C. 102(a) as being anticipated by Ransijn (US 6,392,457 B1).

Regarding **claims 11-12 & 13-14**, in Fig.5, Ransijn discloses a phase detection device (22), comprising:

a clock generator (D4) to generate a measurement clock signal (CK1) having a phase control value related to a reference clock signal (CK2/CLOCK);

a calibration logic (16) to vary the phase control value to provide a predetermined phase relationship between the measurement clock signal (CK1) and a received clock signal (DATA IN), wherein the calibration logic varies the phase control value (CK2/CLOCK) until the phase of the measurement clock signal (CK1) is approximately equal to the phase of the reference clock signal (CK2/CLOCK, column 5, lines 27-30);

an evaluation logic (18) to evaluate the phase control value to detect a phase relationship (FIG.6) between the received clock signal (DATA IN) and the reference clock signal (CK2/CLOCK).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 7 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Brandt (US 5,859,550).

Regarding **claims 2** & **7**, the APA does not show the process, voltage, and temperature (PVD) circuit; however, Brandt teaches the PVD compensated circuit (500) in the clock distribution system in FIG.4. Since, the PVD variation is prevail in the clock distribution system, in order to synchronize the clocks/dart, it would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the PVT-compensated circuit taught by Brandt in the device of APA that the PVT-compensated circuit takes the output of the Phase detection circuit 31 receiving CLKI and CLK2 as inputs to compensate the process, voltage, and temperature variation for the purpose to reduce the clock skew and get accurate clock signals (column 4 lines 20-25 '550).

Regarding **claims 21** & **23**, in Fig.2, the APA discloses a device and its method,

the device comprising a *clock generator* element 22 with PHASE1 setting to generate CLK1 clock signal having phase PHASE1 set relative to the reference clock source 20, a *delay element* 33 of the *calibration logic* (Phase detection circuit 31) delaying the CLK1 wherein the delay element is subject to PVT variation, but the APA does not specify the PVT adjustment.

However, in FIG. 4, Brandt teaches the PVT-compensated circuit in the clock distribution tree of an ASIC interface chip (column 5, lines 23-25 '550) of digital electronic circuitry providing the digital PVT adjustment value. It would have been obvious to a one of ordinary skill in the art at the time the invention was make to have the PVT-sensitive circuit of an ASIC interface chip taught by Brandt in the APA's device that the PVT takes the delayed CLK1 from the output of element 33 and CLK2 of the calibration logic (Phase detection circuit 31) as inputs in response to the phase difference of the two clock signals in a digital form to compensate the process, voltage, and temperature variations for the purpose to reduce the clock skew and get accurate clock signals (column 4, lines 20-25). This modified device has the PVT circuit being responsive to the PVT digital adjustment value which is the output of the element 510 Phase Detector (FIG.5 '550) to compensate the variations.

Regarding **claims 22** & **24**, the APA teaches setting PHASE1 such that the CLK1 having a phase relationship related to the phase of the clock source 20, and the relationship being approximately equal to as choice.

10. Claims 4-5, 9-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Ransijn (US 6,392,457 B1).

Regarding **claims 4 & 9**, in Fig.2, the APA discloses a device comprising a calibration logic (25) to receive a third clock signal (DATAIN having a clock period), however, APA does not explicitly specify the calibration logic to set the second digital control value CLK2 (or CLK1 depending which one is the first and the second).

Ransijn teaches a Phase Detector 22 in FIG.5, receiving a third clock signal (DATA IN) and to set a digital control value (CLOCK/CK1, column 5, lines 11-20 '457).

As APA disclosing the PHASE1 being set might vary during operation, as data is received from different devices with different propagation delays (page 2, lines 15-17, the specification), at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have the calibration logic taught by Ransijn (22 in FIG.5 '457) implemented in the device of APA (Fig.2) as the Phase Detection Circuit 31 and, the logic circuit 25 with its associated logic circuits to receive a third clock signal (DATAIN) and to set the other digital control value PHASE1 or PHASE 2 (CK1) whichever does control the third clock signal DATAIN to adjust the clock phase to synchronize the data. This combination/modification provides a phase detector being substantially proportional to a local clock phase can be produced superior phase jitter performance as well as frequency detection capability (column 5, lines 7-10 '457) that extends the frequency lock range of Phase Lock Loop circuit of the clock recovery circuit (column 1, lines 65-67 '457).

Regarding **claims 5** & **10**, the APA does not explicitly specify calibration logic to vary at least one of the first and second digital control values. However, Ransijn teaches a Phase Detector 22 in FIG.5, receiving a third clock signal (DATAIN) and to set a digital control value (CLOCK/CK1, column 5, lines 11-20 '457).

As APA disclosing the PHASE1 being set might vary during operation, as data is received from different devices with different propagation delays (page 2, lines 15-17, the specification), at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have the calibration logic taught by Ransijn (22 in FIG.5 '457) implemented in the device of APA (Fig.2) as the Phase Detection Circuit 31 and, the logic circuit 25 with its associated logic circuits to receive a third clock signal (DATA IN) and to set the other digital control value PHASE1 or PHASE 2 (CK1) whichever does control the third clock signal DATAIN to adjust the clock phase to synchronize the data. This combination/modification provides a phase detector being substantially proportional to a local clock phase can be produced superior phase jitter performance as well as frequency detection capability (column 5, lines 7-10 '457) that extends the frequency lock range of Phase Lock Loop circuit of the clock recovery circuit (column 1, lines 65-67 '457).

Regarding **claims 15** & **18**, in Fig.2, the APA discloses a device comprising:

a plurality of clock generators, elements 20 & 22 with PHASEI setting to generate the CLK1 with phase having set to a digital control value (PHASE1) and elements 20 & 23 with another digital control value (PHASE2) setting to generate the CLK2 with phase having set PHASE2 value (page 1 line 25-page 2 line 2 APA);

a calibration logic (the phase detection 31) deriving correction values (on 30) producing the phase difference/relationship (page 3, lines 6-12 APA) to produce phase difference;

However, the APA does not explicitly specify the calibration logic to vary the digital control values. Ransijn teaches a Phase Detector 22 in FIG.5, with a plurality clock signals (in DATA IN, CK2, CK1 & CLOCK) and to set the digital control values (CK2, CK1 & CLOCK, column 5, lines 11-20 '457).

As APA disclosing the PHASE1 being set might vary during operation, as data is received from different devices with different propagation delays (page 2, lines 15-17, the specification), at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have the calibration logic taught by Ransijn (22 in FIG.5 '457) implemented in the device of APA (Fig.2) as the Phase Detection Circuit 31 and, the logic circuit 25 with its associated logic circuits to receive a third clock signal (DATA IN) and to set the digital control values PHASE1 or PHASE 2 (CK1 or CK2) to adjust the clock phases to synchronize the data. This combination/modification provides a phase detector being substantially proportional to a local clock phase can be produced superior phase jitter performance as well as frequency detection capability (column 5, lines 7-10 '457) that extends the frequency lock range of Phase Lock Loop circuit of the clock recovery circuit (column 1, lines 65-67 '457).

Regarding **claims 16** & **19**, in Fig.2, the APA discloses the clock signals having approximately identical phases when choosing the phase relationship (element 33) by setting/deriving the control value.

Regarding **claims 17 & 20**, the APA discloses one common reference clock 20.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pan (US 6,348,823 B1) describes a Phase Detector to vary/control the phase values of the clock signals generated (e.g. FIGURE 6).

Stark et al. (US 6,987,823 B1) describes a system and its method for ailigning two or more clock domains.

Zerbe et al. (US 6,949,958 B2) describes circuits for synchronizing data transfer between clock domains of different phases.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed H. Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
April 6, 2006

KHAI TRAN
PRIMARY EXAMINER